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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,158	04/13/2004	Fu-Liang Yang	TSM03-0929	4551

43859 7590 12/29/2005

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EXAMINER	
DOAN, THERESA T	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/823,158	YANG ET AL.	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *19-37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of 1-18 in the reply filed on 10/20/05 is acknowledged.

Information Disclosure Statement

2. The prior art documents submitted by applicant in the Information Disclosure Statement filed on 10/18/04, have all been considered and made of record (note the attached copies of form PTO-1449).

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 14 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- In claim 14, a phrase of "the first thickness is less than about 400 Å, and the second thickness of greater than about 100 Å" is unclear. It is unclear because as recited in independent claim 13, "the second thickness being larger than the first thickness". However, the second thickness of about 100 Å is not greater than the first thickness of about 400 Å (as recited in dependent claim 14).

- Similarly, claim 17 is also unclear because of the same reasons above.

Drawings

5. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-3, 6-11 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Doris et al. (U.S. Pat. 6,911,383).

Regarding claims 1 and 13, Doris (Figs. 10-14) discloses a semiconductor device comprising:

an insulator layer 14 (column 4, lines 37-41);

a planar transistor 34 formed on a first portion of a semiconductor layer 16, the first portion of the semiconductor layer 16 overlying the insulator layer 14, and the first portion of the semiconductor layer 16 having a first thickness h_2 (Fig. 10, column 6, lines 62-65) and

a multiple-gate transistor 32 formed on a second portion of the semiconductor layer 16, the second portion of the semiconductor layer 16 overlying the insulator layer 14, the second portion of the semiconductor layer 16 having a second thickness h_1, and the second thickness h_1 being larger than the first thickness h_2 (Fig. 10, column 6, lines 62-66 and column 7, lines 23-26).

Regarding claim 2, Doris further discloses that the semiconductor layer 16 comprises a material selected from a group consisting of silicon, germanium, silicon germanium, and combinations thereof (column 4, lines 46-49).

Regarding claim 3, Doris (Fig. 10) discloses that the insulator layer 14 comprises silicon oxide (column 4, lines 55-58).

Regarding claim 6, Doris discloses that the planar transistor 34 comprises: a planar channel 34 formed from the first portion of the semiconductor layer 16 (column 6,

lines 62-65); a gate dielectric 40 overlying at least a portion of the planar channel 34 (Fig. 11, column 7, lines 54-56); a gate electrode (42,46) overlying the gate dielectric 40 (Figs. 12-13, column 7, lines 57-67 and column 8, lines 1-7); and source and drain regions (not shown) formed in the first portion of the semiconductor layer 16 oppositely adjacent the gate electrode 46 (column 8, lines 45-49).

Regarding claim 9, Doris discloses that the multiple-gate transistor 32 comprises: a vertical semiconductor fin formed from the second portion of the semiconductor layer 16 (Fig. 10, column 6, lines 62-67); a gate dielectric 40 at least partially wrapping around a channel portion of the fin 16 (Fig. 11, column 7, lines 39-42); a gate electrode (42,44) overlying the gate dielectric 40 (Figs. 12-13, column 7, lines 57-67 and column 8, lines 1-7); and source and drain regions (not shown) formed in the second portion of the semiconductor layer 16 oppositely adjacent the gate electrode 44 (column 8, lines 45-49).

Regarding claims 7 and 10, Doris (Fig. 10) discloses that the gate dielectric 40 comprises a material selected from a group consisting of silicon oxide and silicon oxynitride (column 7, lines 42-46).

Regarding claims 8 and 11, Doris (Fig. 10) discloses that the gate electrode (42,46) comprises a material selected from a group consisting of a metal, a metallic silicide, polysilicon, and combinations thereof (column 7, lines 63-67).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 4-5, 14-15 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doris et al. (U.S. Pat. 6,911,383).

Regarding claims 4-5 and 14, Doris does not disclose that the first thickness is less than about 400 Å and the second thickness is greater than about 100 Å.

However, Doris's Fig. 10 teaches the thickness of the top semiconductor layer 16 is about 100 to 1000 Å (column 5, lines 6-7) and an optional thinning step may follow the bonding process. The optional thinning step reduces the thickness of the top semiconductor 16 to a layer having a thickness that is more desirable (column 5, lines 2-5). It has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233.* Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the first and second thickness of Doris by forming the first thickness is less than about 400 Å and the second thickness is greater than about 100 Å because the changes in thickness of semiconductor layer for the first thickness and the second thickness can be varied depending upon the size that desired for the semiconductor device such as a planar transistor or a multiple-gate transistor.

Regarding claim 17, Doris (Figs. 10-14) discloses a semiconductor device comprising: an insulator layer 14 (column 4, lines 37-41); a first portion of a semiconductor layer 16 having a first thickness h_2 (Fig. 10, column 6, lines 62-65), the first portion of the semiconductor layer 16 overlying the insulator layer 14; a second portion of the semiconductor layer 16 having a second thickness h_1, the second portion of the semiconductor layer 16 overlying the insulator layer 14, and the second thickness h_1 being larger than the first thickness h_2 (Fig. 10, column 6, lines 62-66 and column 7, lines 23-26); a first transistor 34 having a first active region formed from the first portion of the semiconductor layer; and a second transistor 32 having a second active region formed from the second portion of the semiconductor layer 16 (Fig. 10, column 6, lines 62-66 and column 7, lines 23-26).

Doris does not disclose that the first thickness is less than about 400 Å and the second thickness is greater than about 100 Å.

However, Doris's Fig. 10 teaches the thickness of the top semiconductor layer 16 is about 100 to 1000 Å (column 5, lines 6-7) and an optional thinning step may follow the bonding process. The optional thinning step reduces the thickness of the top semiconductor 16 to a layer having a thickness that is more desirable (column 5, lines 2-5). It has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233.* Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the first and

second thickness of Doris by forming the first thickness is less than about 400 Å and the second thickness is greater than about 100 Å because the changes in thickness of semiconductor layer for the first thickness and the second thickness can be varied depending upon the size that desired for the semiconductor device such as a planar transistor or a multiple-gate transistor.

Regarding claims 15 and 18, Doris (Fig. 10) discloses that the first transistor 34 is a planar transistor, and the second transistor 32 is a multiple-gate transistor.

10. Claims 12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doris et al. (U.S. Pat. 6,911,383) in view of Hieda (US 2002/0011612).

Doris does not disclose that corners of the semiconductor layer are rounded at edges of active regions of the planar and multiple-gate transistors.

However, Hieda (Figs. 28 and 66) teaches a semiconductor device having a rounded top corner channel semiconductor layer 15 (paragraph [0187]), as shown in Fig. 28, the influence of the electric field from the gate electrode 16 can be remarkable decreased (see paragraphs [0318] to [0320]). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the device of Doris by forming the corners of the semiconductor layer are rounded at edges of active regions of the planar and multiple-gate transistors because such a forming structure of a round of the top corner of the semiconductor layer would decrease the

influence of the electric field from the gate electrode and the pressure endurance of the gate insulating can be improve, as taught by Hieda (see paragraphs [0318] to [0320]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Theresa Doan
Patent Examiner
December 12, 2005.